Electronic Version
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Claims

[c1] 1. A quad flat no-lead chip carrier, comprising:
a conductive plate having a first surface and a second surface, wherein the first surface has a chip-bonding region and the conductive plate furthermore has a plurality of columnar through holes located on the periphery of the chip-bonding region such that the columnar through holes pass through the conductive plate to link up the first and the second surfaces;
a plurality of conductive columns set up within the respective columnar through holes; and
a plurality of dielectric walls set up between the sidewall of the conductive columns and the inner surface of corresponding columnar through holes.

[c2] 2. The chip carrier of claim 1, wherein the first surface of the conductive plate is a rough surface.

[c3] 3. The chip carrier of claim 1, wherein the first surface of the conductive plate has an oxide layer thereon.

[c4] 4. The chip carrier of claim 1, wherein the carrier further comprises a solder mask layer set up on the second surface of the conductive plate that exposes a portion of an

end surface of the conductive columns near the second surface.

[c5] 5. A quad flat no-lead chip package, comprising:
a chip carrier comprising:
a conductive plate having a first surface and a second surface, wherein the first surface has a chip-bonding region and the conductive plate furthermore has a plurality of columnar through holes located on the periphery of the chip-bonding region such that the columnar through holes pass through the conductive plate to link up the first and the second surface;
a plurality of conductive columns set up within the respective columnar through holes; and
a plurality of dielectric walls set up between the sidewall of the conductive columns and the inner surface of corresponding columnar through holes;
a chip attached to the chip-bonding region on the first surface of the conductive plate;
a plurality of first conductive wires electrically connecting the chip and the conductive columns; and
an insulating material enclosing the chip and the first conductive wires.

[c6] 6. The chip package of claim 5, wherein the package further comprises at least a second conductive wire electrically connecting the chip to the conductive plate.

[c7] 7. The chip package of claim 5, wherein the package further comprises a conductive paste layer sandwiched between the chip and the conductive plate.

[c8] 8. The chip package of claim 5, wherein the first surface of the conductive plate is a rough surface.

[c9] 9. The chip package of claim 5, wherein the first surface of the conductive plate has an oxide layer thereon.

[c10] 10. The chip package of claim 5, wherein the carrier further comprises a solder mask layer set up on the second surface of the conductive plate that exposes a portion of an end surface of the conductive columns near the second surface.